**Project 4**

Develop your VHDL code for the following problems and simulate it as instructed.

Submit your project folder and the screen shots of the results.

(a) Write a behavioral VHDL description of the state machine that you designed in Problem 1.14. Generated state table is given here. Assume that state changes occur on the falling edge of the clock pulse. Use a case statement together with if-then-else statements to represent the state table.

1. Write a testbench to test your code. The code should include the state machine as a component. You test code should generate a clock with 20 ns period. The code should apply the following test sequence:

X=010011101010101101

X should change 5 ns after the rising edge of the clock. Your test code should read Z at an appropriate time and report the result of the following output sequences:

1. Z= 000000000011000011 (Must print out a message of “Sequence is correct”)
2. Z= 000000000011010101 (Must identify the wrong numbers in the sequence)

